

239 **CLAIMS**

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241 I claim:

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244 1. In a dynamic random access memory device, having a complementary-logic bitline pair
245 having true and inverted bitlines:

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247 equilibrating means, connected to the bitline pair; and

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249 biasing means, connected to only one of the bitlines;

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251 wherein when said equilibrating and biasing means are activated together, the
252 bitline pair is thus equilibrated and biased.

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255 2. The device of claim 1, wherein:

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257 said equilibrating means comprises a first transistor, connected to the bitline pair,
258 such that when activated, the bitlines are shorted together;

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260 said biasing means comprises a second transistor, connected to only one of the
261 bitlines and connected to a biasing node, such that when activated, the one of said
262 bitlines is shorted to said biasing node;

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264 such that when said first and second transistors are activated together, said bitline
265 pair is equilibrated and biased.

268 3. The device of claim 2, wherein said biasing node is located next to said second
269 transistor.

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272 4. The device of claim 2, wherein said biasing node is connected to a current-limiting
273 device, and wherein an n-channel substrate contact can be located next to said current-
274 limiting device without widening circuit area.

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277 5. The device of claim 2, wherein an n-channel contact can be located next to said biasing
278 node, without widening circuit area.

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281 6. In a dynamic random access memory device, having a biasing node, and first and second
282 complementary-logic bitline pairs each having a true and an inverted bitline:

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284 first equilibrating means, able to short the bitlines of the first bitline pair together;

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286 second equilibrating means, able to short the bitlines of the second bitline pair
287 together;

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289 first biasing means, able to short only one of the bitlines of the first bitline pair to
290 the biasing node;

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292 second biasing means, able to short only one of the bitlines of the second bitline
293 pair to the biasing node;

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295 wherein the biasing node is interstitially located between said first and second
296 biasing means.

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299 7. The device of claim 6, wherein:

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301 said first equilibrating means comprises a first transistor, connected to the first
302 bitline pair, such that when said first transistor is activated, the first bitline pair is
303 shorted together;

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305 said second equilibrating means comprises a second transistor, connected to the
306 second bitline pair, such that when said second transistor is activated, the second
307 bitline pair is shorted together;

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309 said first biasing means comprises a third transistor, connected to only one of the
310 bitlines in the first bitline pair and connected to a biasing node, such that when said
311 third transistor is activated, the one of said bitlines of the first bitline pair is shorted
312 to said biasing node;

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314 said second biasing means comprises a fourth transistor, connected to only one of
315 the bitlines in the second bitline pair and connected to said biasing node, such that
316 when said fourth transistor is activated, the one of said bitlines of the second bitline
317 pair is shorted to said biasing node;

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319 wherein said first, second, third, and fourth transistors are activated together, thus
320 equilibrating and biasing the bitline pair.

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323 8. The device of claim 7, wherein said biasing node is connected to a current-limiting
324 device, and wherein an n-channel substrate contact can be located next to said current-
325 limiting device without widening circuit area.

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328 9. The device of claim 7, wherein an n-channel contact can be located next to said biasing
329 node, without widening circuit area.

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332 10. In a dynamic random access memory device, having:

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334 an equilibrate node;

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336 a biasing node;

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338 a complementary-logic bitline pair having true and inverted bitlines;

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340 a first transistor, connected to said bitline pair and gated by said equilibrate node
341 such that when said equilibrate node is activated, said bitline pair is shorted
342 together and thus equilibrated;

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344 a second transistor, connected to said true bitline and to said biasing node, and
345 gated by said equilibrate node, such that when said equilibrate node is activated,
346 said true bitline is shorted to said biasing node, thus biasing said true bitline;

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348 a third transistor, connected to said inverted bitline and to said biasing node, and
349 gated by said equilibrate node, such that when said equilibrate node is activated,
350 said inverted bitline is shorted to said biasing node, thus biasing said inverted
351 bitline;

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353 the improvement comprising:

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355 conversion of one of said second and third transistors from a three-terminal device
356 to a two-terminal device, allowing said biasing node to be located next to

remaining unconverted of said second and third transistors, without widening circuit area.

11. The device of claim 10, wherein said biasing node is connected to a current-limiting device, and wherein an n-channel substrate contact can be located next to said current-limiting device without widening circuit area.

12. The device of claim 10, wherein an n-channel contact can be located next to said biasing node, without widening circuit area.

13. In a dynamic random access memory device, having:

an equilibrate node;

a biasing node;

a complementary-logic bitline pair having true and inverted bitlines;

a first transistor, connected to said bitline pair and gated by said equilibrate node such that when said equilibrate node is activated, said bitline pair is shorted together and thus equilibrated;

a second transistor, connected to said true bitline and to said biasing node, and gated by said equilibrate node, such that when said equilibrate node is activated, said true bitline is shorted to said biasing node, thus biasing said true bitline;

386 a third transistor, connected to said inverted bitline and to said biasing node, and
387 gated by said equilibrate node, such that when said equilibrate node is activated,
388 said inverted bitline is shorted to said biasing node, thus biasing said inverted
389 bitline;

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391 the improvement comprising:

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393 elimination of one of said second and third transistors, allowing said biasing node
394 to be located next to remaining of said second and third transistors, without
395 widening circuit area.

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398 14. The device of claim 13, wherein said biasing node is connected to a current-limiting
399 device, and wherein an n-channel substrate contact can be located next to said current-
400 limiting device without widening circuit area.

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403 15. The device of claim 13, wherein an n-channel contact can be located next to said
404 biasing node, without widening circuit area.